

# Online Research @ Cardiff

This is an Open Access document downloaded from ORCA, Cardiff University's institutional repository: <https://orca.cardiff.ac.uk/id/eprint/135927/>

This is the author's version of a work that was submitted to / accepted for publication.

Citation for final published version:

Abdullah, Isam, Macdonald, J Emyr ORCID: <https://orcid.org/0000-0001-5504-1692>, Lin, Yen-Hung, Anthopoulos, Thomas D, Hma Salah, Nasih, AnwarKakil, Shaida and Muhammedsharif, Fahmi F 2020. Bias stability of solution-processed In<sub>2</sub>O<sub>3</sub> thin film transistors. Journal of Physics: Materials 4 , 015003. 10.1088/2515-7639/abc608 file

Publishers page: <https://doi.org/10.1088/2515-7639/abc608>  
<<https://doi.org/10.1088/2515-7639/abc608>>

Please note:

Changes made as a result of publishing processes such as copy-editing, formatting and page numbers may not be reflected in this version. For the definitive version of this publication, please refer to the published source. You are advised to consult the publisher's version if you wish to cite this paper.

This version is being made available in accordance with publisher policies.

See

<http://orca.cf.ac.uk/policies.html> for usage policies. Copyright and moral rights for publications made available in ORCA are retained by the copyright holders.



PAPER • OPEN ACCESS

## Bias stability of solution-processed $\text{In}_2\text{O}_3$ thin film transistors

To cite this article: Isam Abdullah *et al* 2021 *J. Phys. Mater.* **4** 015003

View the [article online](#) for updates and enhancements.

# 239th ECS Meeting

with the 18th International Meeting on Chemical Sensors (IMCS)

**ABSTRACT DEADLINE: DECEMBER 4, 2020**



May 30-June 3, 2021

**SUBMIT NOW →**



## PAPER

## OPEN ACCESS

RECEIVED  
18 July 2020

REVISED  
16 October 2020

ACCEPTED FOR PUBLICATION  
29 October 2020

PUBLISHED  
17 November 2020

Original content from  
this work may be used  
under the terms of the  
[Creative Commons  
Attribution 4.0 licence](#).

Any further distribution  
of this work must  
maintain attribution to  
the author(s) and the title  
of the work, journal  
citation and DOI.

Bias stability of solution-processed  $\text{In}_2\text{O}_3$  thin film transistors

Isam Abdullah<sup>1</sup> , J Emyr Macdonald<sup>2</sup> , Yen-Hung Lin<sup>3,4</sup> , Thomas D Anthopoulos<sup>3,5</sup> ,  
Nasih Hma Salahr<sup>1</sup>, Shaida Anwar Kakil<sup>1</sup> and Fahmi F Muhammadsharif<sup>6</sup>

<sup>1</sup> Department of Physics, College of Science, Salahaddin University-Erbil, Erbil, Iraq

<sup>2</sup> School of Physics and Astronomy, Cardiff University, The Parade, Cardiff CF24 3AA, United Kingdom

<sup>3</sup> Department of Physics and Centre for Plastic Electronics, Blackett Laboratory, Imperial College London, London, United Kingdom

<sup>4</sup> Clarendon Laboratory, Department of Physics, University of Oxford, Oxford OX1 3PU, United Kingdom

<sup>5</sup> King Abdullah University of Science and Technology (KAUST) Solar Center (KSC), Division of Physical Sciences and Engineering,  
King Abdullah University of Science and Technology (KAUST), Thuwal 23955-6900, Saudi Arabia

<sup>6</sup> Department of Physics, Faculty of Science and Health, Koya University, 44023 Koya, Iraq

E-mail: [macdonald@cardiff.ac.uk](mailto:macdonald@cardiff.ac.uk)

**Keywords:** solution processed, indium oxide TFTs, bias stress, threshold voltage

Supplementary material for this article is available [online](#)

## Abstract

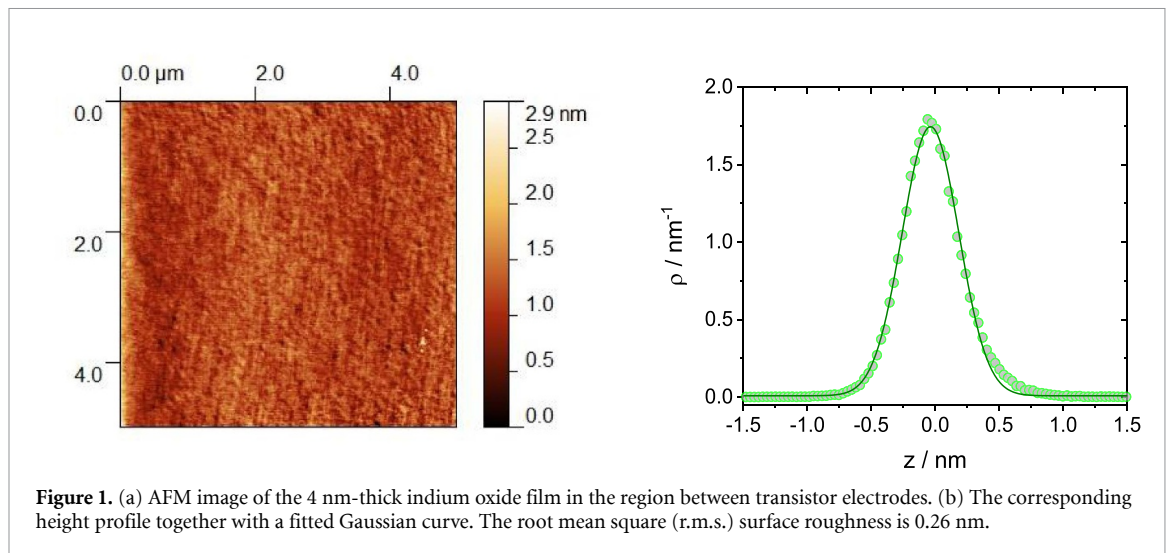
We report the effect of bias stress on the drain current and threshold voltage of n-channel thin-film transistors based on solution processed  $\text{In}_2\text{O}_3$  layers. Application of a positive gate bias for variable time-periods led to displacements of the transfer curves in the positive gate bias direction. On switching off the gate bias, the transfer curves returned close to their pre-stress state on a timescale similar to that when the gate bias was switched on. The time dependence of the threshold voltage shift is described well by a stretched-exponential model. The temporal behaviour of the threshold voltage shifts is consistent with charge trapping as the dominant effect, although some defect formation cannot be ruled out.

## 1. Introduction

In recent years, transparent oxide thin film transistors (TFTs) have been extensively studied due to their high-performance and potential use in various low-effective technological application [1–6]. Recent investigations demonstrated the key properties of oxide TFTs, including device mobility [6], film uniformity over large areas [7], high optical transparency in the visible region [8], low off-current and compatibility with various fabrication methods [9, 10]. The development of large-area, low cost devices relies strongly on the fabrication methods and the choice of materials [11, 12]. A number of metal-oxide based TFTs such as indium oxide ( $\text{In}_2\text{O}_3$ ), indium zinc oxide (IZO), and indium gallium zinc oxide (IGZO) have demonstrated high mobilities and reasonable device performance at low or room temperature, using different device dimensions and various fabrication methods [13–16].

$\text{In}_2\text{O}_3$  is one of the most important and promising semiconductor materials for such applications due to its wide band gap, high symmetry cubic structure, phase purity and low cost [17].  $\text{In}_2\text{O}_3$  has been effectively prepared by various techniques, such as magnetron sputtering [18], electro-spinning [5, 19], atomic layer deposition [6, 20, 21] pulsed laser deposition [22, 23] and spray pyrolysis [7]. One of the key issues for  $\text{In}_2\text{O}_3$  thin-film devices is the stability of the threshold voltage after prolonged application of gate voltage, referred to as bias stress [24, 25].

Due to the attractiveness of its use in recent electronic devices, it is crucial to understand the key mechanisms that influence the performance and stability of the solution-processed metal oxide TFTs. We report an experimental investigation of the effect of bias stress effect on top-contact bottom-gate  $\text{In}_2\text{O}_3$  device stability over prolonged bias stress. Device recovery after stress release and possible mechanisms of bias stress and recovery are discussed in the context of our experimental data.



## 2. Experimental procedure

The  $\text{In}_2\text{O}_3$  precursor solution was prepared by dissolving anhydrous indium nitrate [ $\text{In}(\text{NO}_3)_3$ ] (99%, Indium Corporation) in deionized water at a concentration of  $30 \text{ mg ml}^{-1}$ . The solution was stirred at room temperature for 60 min before use. For the fabrication of low-temperature aqueous-based  $\text{In}_2\text{O}_3$  TFT, the semiconductor thin-film deposition was carried out by spin-casting the  $\text{In}_2\text{O}_3$  precursor solution onto highly doped Si substrates having a 100 nm thermally grown  $\text{SiO}_2$  gate dielectric layer at 3000 rpm for 30 s under ambient conditions, followed by a post-deposition thermal anneal process for 30 min at  $200^\circ\text{C}$ . Procedures used for preparing and characterizing the films are described in [7, 26].

40 nm-thick Al top source and drain electrodes were deposited through a shadow mask. The sample size was  $2 \text{ cm} \times 2 \text{ cm}$ , and each sample included 98 devices. Where required, samples were cleaved to access fewer devices for use in the atomic force microscope (AFM). Transistors were bonded with gold wire of diameter 0.06 mm with conductive silver paint (Silverdag, Agar Scientific) under an optical microscope. Devices having channels of varying length ( $L$ ) and width ( $W$ ) were prepared and stored under vacuum to prevent degradation. Device current–voltage ( $I$ – $V$ ) data were recorded with a Keithley Picoammeter-6487, controlled using a python script. Scanning probe microscopy images were performed using a Bruker Multimode instrument in intermittent contact mode.

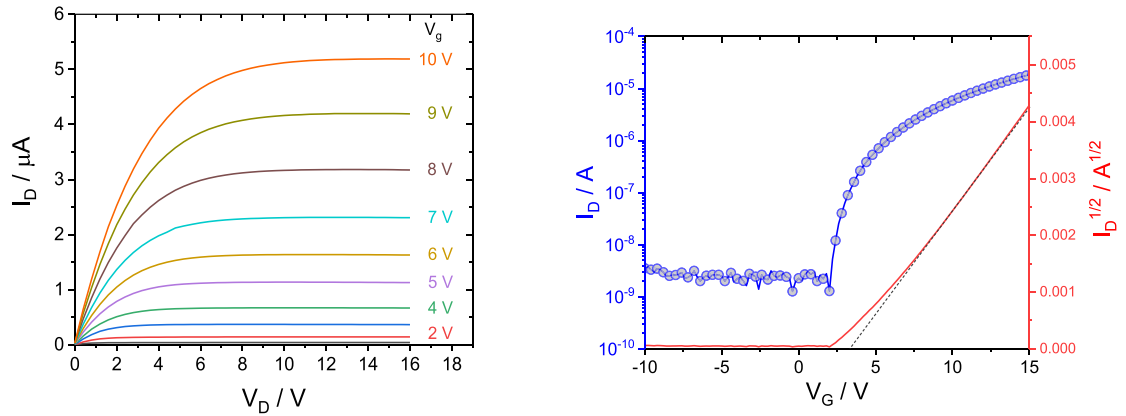
## 3. Results and discussion

As-grown films are found to be highly transparent across the entire visible spectrum (i.e. 400–700 nm), with an average transmittance of more than 95% (substrate-corrected values). A sharp absorption characteristic was observed in the UVA region as expected from the wideband gap property of indium oxide owing to its electronic inter-band transition (figure S1, supplementary information (<https://stacks.iop.org/JPMATER/4/015003/mmedia>)). AFM measurements were performed in intermittent contact mode to examine the surface morphology, as shown in figures 1(a) and (b), giving a root-mean-square surface roughness ( $\sigma_{\text{rms}}$ )

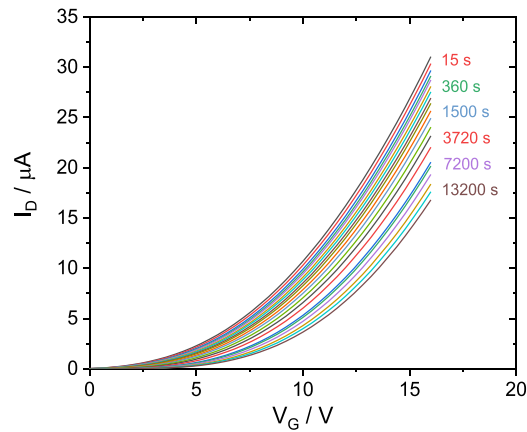
In terms of quantifying the performance of the transistor channel layer, the most important TFT property is its output and transfer characteristics. Figures 2(a) and (b) show a set of representative transfer and output characteristics of an  $\text{In}_2\text{O}_3$  TFT of channel thickness 4 nm with channel width ( $W$ ) and length ( $L$ ) of  $1000 \mu\text{m}$  and  $30 \mu\text{m}$ , respectively. The source-to-drain current increase with increasing gate-source bias due to electron accumulation at the  $\text{In}_2\text{O}_3/\text{SiO}_2$  interface. The device shows excellent pinch-off characteristics, which indicates that electron transport in the channel is fully controlled by drain and gate bias. Furthermore, the device exhibits clear current–voltage modulation with drain current on-off ratio of nearly  $10^5$  and  $V_{\text{th}} = 2.1 \text{ V}$  operating in accumulation mode in positive gate bias. The obtained saturation mobilities are in the range of  $0.2$ – $0.3 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  with n-type semiconductor behavior.

The electrical stability of TFTs is important for stable display performance. Bias stress instability leads to threshold voltage shift with time during application of gate voltage, which in turn causes a decrease in drain current. Therefore, the generation and recovery of these instabilities over time may lead to time-dependent operation of the device, followed eventually by dysfunction. Bias stress can potentially lead to instabilities





**Figure 2.** (a) The output characteristic for a  $\text{In}_2\text{O}_3$  transistor (film thickness 4 nm,  $W = 1000 \mu\text{m}$ ,  $L = 30 \mu\text{m}$ ). The applied gate bias was incremented in 1 V steps from  $V_G = 1 \text{ V}$  to  $V_G = 10 \text{ V}$ . (b) The corresponding transfer characteristics at  $V_D = 10 \text{ V}$ . The resulting values for  $V_{th}$  and  $\mu_{sat}$  are  $(2.07 \pm 0.12) \text{ V}$  and  $0.22 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  respectively.



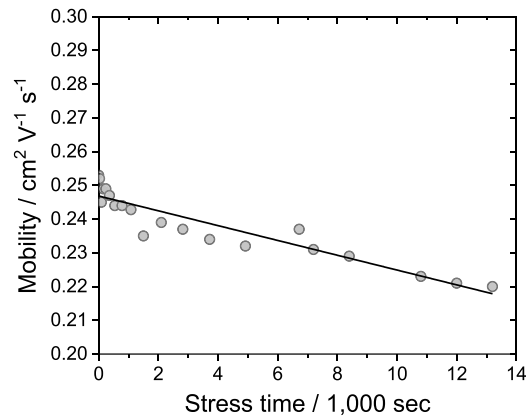
**Figure 3.** Transfer characteristic curves shift with stressing time of  $W = 1000 \mu\text{m}$  and  $L = 30 \mu\text{m}$ . The drain bias was 10 V and the stressing gate bias was maintained at 10 V for stress time durations of 0, 15, 30, 90, 150, 240, 360, 540, 780, 1080, 1500, 2100, 2820, 3720, 4920, 6720, 7200, 8400, 10 800, and 13 200 s.

such as charge trapping, defects in the active channel layer, in the gate dielectric, and at the active layer/dielectric interface. Mechanisms for such degradation have been proposed. For instance, Nomura *et al* [27] in the study of a-In-Ga-Zn-O suggested that shallow traps are the origin of large threshold voltage shift ( $\sim 10 \text{ V}$ ) and subthreshold deterioration observed in unannealed devices, while deep traps are responsible for small shifts ( $\sim 1 \text{ V}$ ), not removed by annealing. On the other hand, Lei *et al* (2008) and Suresh *et al* (2008) [25, 28] attributed degradation to charge trapping in the channel/dielectric interface and bulk semiconductor. Strategies to mitigate carrier trapping and reduce the associated bias-stress have also been reported [29].

With the source electrode grounded and the drain bias fixed at 10 V, the gate bias was applied for an extended period, with regular interruptions, each of 5 s, to record the transfer characteristics for a sweep of  $V_G$  from  $-5 \text{ V}$  to  $16 \text{ V}$ . The quoted stressing time is the cumulative time during which the bias stress was applied. Figure 3 shows a set of transfer curves of a TFT transistor having channel width and length of  $1000 \mu\text{m}$  and  $30 \mu\text{m}$  respectively. Transfer curves for different stressing times reveal progressive shifts toward larger threshold voltages. The positive shifts of threshold voltage with stress time could be due to electron trapping at the channel/dielectric interface or injected into the dielectric or creation of defect states at or close to the channel/insulator interface [24, 29–31].

Trapped electrons at the interface between active layer and oxide dielectric reduce the effective gate bias and consequently shifts the threshold voltage in the positive direction. The lower effective gate bias results in smaller drain current flow through device channel, requiring increased gate bias to switch on the device and reach saturation [21]. The shift in threshold voltage as a function of time  $t$  is

$$\Delta V_{th} = V_{th}(t) - V_{th}(t = 0).$$



**Figure 4.** Variation of mobility with stress time (film thickness 4 nm,  $W = 1000 \mu\text{m}$ ,  $L = 30 \mu\text{m}$ ).

It is well known for a TFT that there are two effects causing instability: defect creation in the channel and charge trapping in the dielectric material and at the channel/insulator interface [24]. Defect creation leads to lasting changes in the sub-threshold slope and device mobility, whereas charge trapping does not [32]. Figure 4 shows the variation of device mobility with stress time, which reveals a slight change in the device mobility over long stress periods.

Charge can be trapped either in the channel or at its interface with the dielectric or by injection into the dielectric. The major difference between charge trapping at the interface and injection into the dielectric is the amount of energy needed to remove the injected charge: higher energy is required to release charge injected into the dielectric, usually requiring thermal annealing or application of bias [33]. Our device dielectric material was 100 nm-thick thermally grown silicon dioxide which has a low density of bulk trap states so the fact that the device recovers quickly without annealing indicates that transient charge trapping or induced states are mainly involved.

The threshold voltage shift observed for our indium oxide TFTs can be well described as a function of time  $t$  with the stretched exponential equation [28, 34].

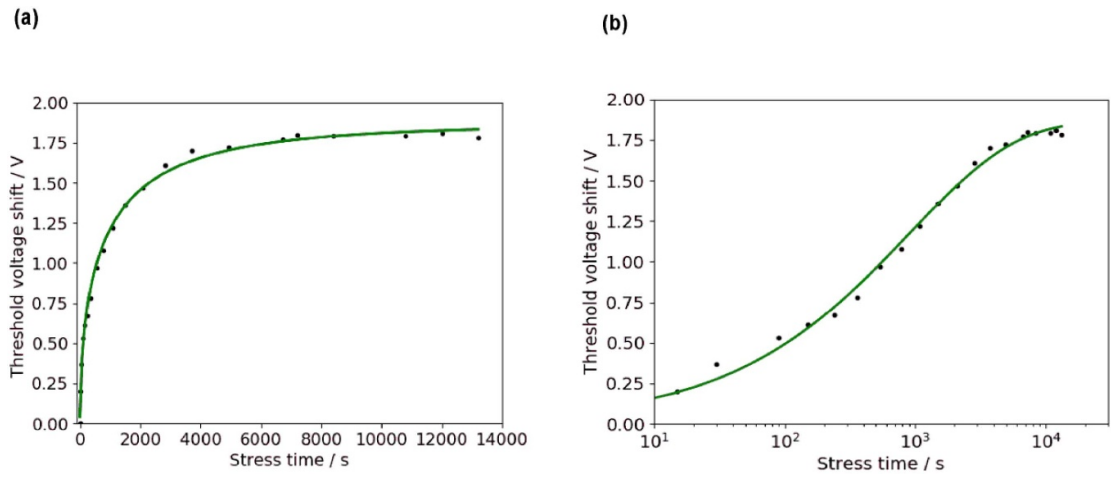
$$\Delta V_{\text{th}}(t) = \Delta V_{\text{th}0} [1 - \exp[-(t/\tau)^\beta]], \quad (1)$$

where  $\Delta V_{\text{th}0} = [V_{\text{th}}(t \rightarrow \infty) - V_{\text{th}}(t = 0)]$ . Here,  $0 < \beta < 1$  is the stretched function exponent and  $\tau$  represents the characteristic trapping time (time constant) which correlates with the average effective energy barrier. Equation (1) is an empirical function introduced by Rudolf Kohlrausch in 1854 to describe the time dependent discharge of a capacitor, sometimes known as the Kohlrausch function. The exponent  $\beta$  describes the degree of deviation from an exponential function. When  $\beta$  is close to unity, it indicates a narrow distribution of time constants, the limiting value of 1 corresponding to a single time constant. Smaller values of  $\beta < 1$  imply a broader distribution of time constants [35]. Figures 5(a) and (b) shows the fitting of threshold voltage shift with stressing time according to equation (1) on both a linear and a logarithmic scale.

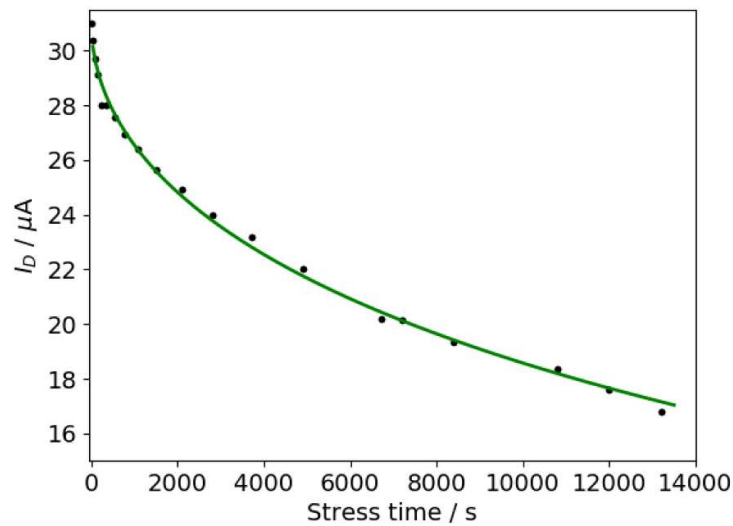
The experimental data of the threshold voltage shift with stressing time agree well with the stretched exponential function presented in equation (2) and the extracted fitting parameters from curve fitting are  $\Delta V_{\text{th}0} = 1.86 \pm 0.06 \text{ V}$ ,  $\beta = 0.53 \pm 0.14$ , and  $\tau = (3.64 \pm 0.23) \times 10^4 \text{ s}$ . Based on the gradual channel model and the stretched exponential function of  $\Delta V_{\text{th}}$ , the drain current can be written as [36].

$$\frac{I_d(t)}{I_d(t=0)} = \exp[-(t/\tau)^\beta] \quad (2)$$

Figure 6 shows the time-dependent drain current under positive stress. The reduction in current with stress time is clear with a fast initial decrease and a slow decrease at extended time without establishing a steady state. After the gate bias was switched off, the current recovery was rapid in the first few seconds but slows thereafter. The measured drain current under varied stressing time also agreed with equation (2), giving fitting parameters  $\beta = 0.52 \pm 0.11$ ,  $\tau = (3.60 \pm 0.16) \times 10^4 \text{ s}$ , consistent with those obtained from the fit to the threshold voltage shift. As noted, in common with many experimental studies of bias stress, the threshold voltage shift as a function of stressing time was monitored by regular transfer characteristics. Ideally, the bias stress should be applied without such interruptions in which  $V_G$  is swept repeatedly. Each sweep of  $V_G$  took 5 s, during which it is estimated that the threshold voltage shift reduced by  $\sim 0.04 \text{ V}$ , about 2% of  $\Delta V_{\text{th}0}$ . The cumulative effect of such partial stress relaxations may influence the threshold voltage



**Figure 5.** Time dependence of the threshold voltage shift under an applied gate bias stress 10 V on a linear scale (left) and logarithmic scale (right). The green lines show the optimized fit of the Kohlrausch function (equation (1)) to the data, the resulting fitted parameters being  $\Delta V_{tho} = 1.86 \pm 0.06$  V,  $\beta = 0.53 \pm 0.14$ , and  $\tau = (3.64 \pm 0.23) \times 10^4$  s.

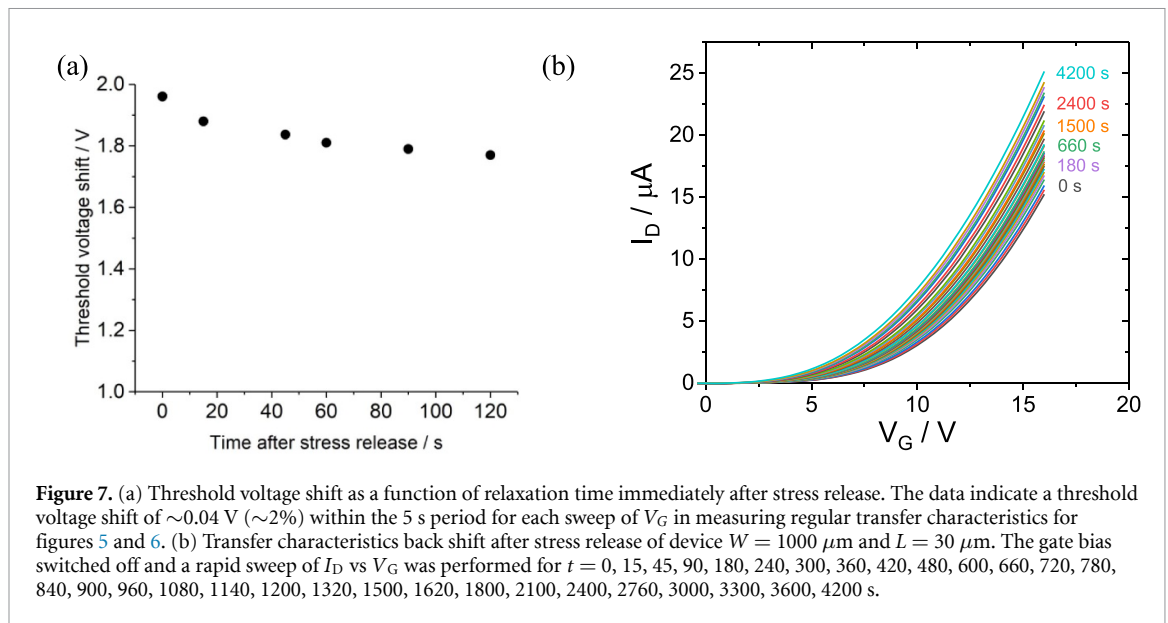


**Figure 6.** Drain current decrease with stress time according to equation (2). The extracted fitting parameters are  $I_{do} = 3.08 \times 10^{-5}$  A,  $\beta = 0.52 \pm 0.11$ , and  $\tau = (3.6 \pm 0.16) \times 10^4$  s.

shifts recorded for extended stress times. The alternative approach of measuring each threshold voltage shift on a singly stressed new sample would considerably increase the experimental effort involved.

The values of the time constant  $\tau$  and the stretching parameter  $\beta$  obtained from these fits are similar to those reported for IGZO. For IGZO, reported values of  $\tau$  are generally in the range 2000–20 000 s [28, 37–39] with occasional reports of values of the order of  $10^5$ – $10^6$  s [40]. The reported values of  $\beta$  for these papers lie in the range 0.4–0.8. Multilayer hybrid  $\text{In}_2\text{O}_3/\text{ZnO}$  nanoparticle TFTs display strong stability to bias stress with a long time constant  $\tau = 2.6 \times 10^8$  s and  $\beta = 0.40$  [41]. (For these multilayers, n-type doping of the Zn nanoparticles with aluminium reduces  $\tau$  to 6000 s with  $\beta = 1.0$  [41], likely related to the lineup of the dopant levels with the conduction band minimum.) Our fitted values indicate that the bias stress behaviour in solution-processed  $\text{In}_2\text{O}_3$  films is similar to that observed in IGZO.

In some electronic applications such as active matrix displays, the TFT is switched on only for limited time, so the resulting shift in threshold voltage relaxes in the off state. Therefore, recovery is as important as stress and the device should return to its original state after stress release. The recovery of  $\Delta V_{th}$  after switching off the bias stress was monitored, and we found that the threshold voltage shift is almost fully reversible and recovered gradually, as seen in figure 7, with  $\Delta V_{th} = 0.17$  V after 4200 s,  $\sim 10\%$  of its value in the stressed state before relaxation. The drain current  $I_D$  after 4200 s is also slightly reduced compared to that at a corresponding  $V_G$  in figure 3. This reversibility indicates that the stress is rapidly and almost fully released when the gate bias switched off.



**Figure 7.** (a) Threshold voltage shift as a function of relaxation time immediately after stress release. The data indicate a threshold voltage shift of  $\sim 0.04$  V ( $\sim 2\%$ ) within the 5 s period for each sweep of  $V_G$  in measuring regular transfer characteristics for figures 5 and 6. (b) Transfer characteristics back shift after stress release of device  $W = 1000 \mu m$  and  $L = 30 \mu m$ . The gate bias switched off and a rapid sweep of  $I_D$  vs  $V_G$  was performed for  $t = 0, 15, 45, 90, 180, 240, 300, 360, 420, 480, 600, 660, 720, 780, 840, 900, 960, 1080, 1140, 1200, 1320, 1500, 1620, 1800, 2100, 2400, 2760, 3000, 3300, 3600, 4200$  s.

Published studies of the effects of bias stress in  $In_2O_3$  films do not report fitting with a stretched exponential function for direct numerical comparison with our results. Vygraneko *et al* [24] measured threshold voltage shifts in  $In_2O_3$  transistors, deposited by reactive ion beam-assisted evaporation, after applying a gate bias of + 10 V for 600 s and after 6000 s—and again 300 s after switching off the gate bias. Their results show broadly similar behaviour to ours, also showing fast recovery without annealing. A puzzling difference is their observation of a slight decrease in the threshold voltage shift for long stress times ( $>3000$  s) whereas our results show an asymptotic approach to a constant value. Lee *et al* [42] compared the electrical stability of solution-processed  $In_2O_3$  devices maintained under vacuum with those maintained in air. Repeated measurements of transfer characteristics showed a slow decrease in mobility in air and a slight increase under vacuum. Larger threshold voltage shifts in air were interpreted by the authors as the result of electrostatic interactions between electrons and polar water molecules at grain boundaries in the nanocrystalline  $In_2O_3$  films [42].

#### 4. Summary and conclusions

We fabricated solution-processed indium oxide TFTs with a top-contact bottom-gate structure exhibiting  $n$ -channel accumulation during operation. The effect of bias-stress measurements on indium oxide based TFT were investigated to check the device stability under prolonged gate bias. Fitting of the stressing time dependence of the threshold voltage shift with a stretched exponential function yields similar values of  $\tau$  and  $\beta$  to those reported for IGZO. The trapping time constant is widely distributed: during the early stages of bias stress, traps of small time constant are initially filled. As the stressing time increases, traps with increasingly higher time constant get filled. Accordingly, a mechanism of wide distribution of time constants should provide either a distribution of energy barriers between majority carriers and traps or both. The rate at which  $V_{th}$  shifts during gate bias stress decreases with time (figure 5), as is observed in metal oxide, organic and amorphous silicon TFTs [34–36, 43–45].

Following bias stress of 10 V applied for 13 200 s, once switched off the threshold shift decreases, reaching around 10% of the value in the stressed state after 4200 s, indicating rapid and relatively complete relaxation during this time period. It suggests that charge trapping is the dominant process rather than defect creation which is irreversible at room temperature, though some defect formation cannot be ruled out. The exact nature and location of charge trapping cannot be unambiguously determined. A recent study comparing devices operated in air and in vacuum has proposed electron binding to water molecules at nanocrystalline grain boundaries in the channel as an alternative trapping mechanism [42]. Thus, future studies should focus on addressing the impact of microstructure on bias-stress stability of the TFTs. A simple way forward would be to study the impact of annealing temperature on  $In_2O_3$  TFT operation, while microstructural analysis of the channel layer via non-destructive techniques, such as x-ray diffraction, could enable a detailed structure-property relationship(s) to be established. There is no doubt that elucidating the key processes responsible for the observed bias-instability in many oxide TFTs could help scientists to develop new



materials and/or mitigation strategies, thus further accelerating the incorporation of the technology in commercial products.

## Acknowledgments

IA acknowledges Salahaddin University for ongoing support. TDA acknowledges the King Abdullah University of Science and Technology (KAUST) for financial support.

## ORCID iDs

Isam Abdullah  <https://orcid.org/0000-0003-3645-1906>  
 J Emyr Macdonald  <https://orcid.org/0000-0001-5504-1692>  
 Yen-Hung Lin  <https://orcid.org/0000-0001-6819-1235>  
 Thomas D Anthopoulos  <https://orcid.org/0000-0002-0978-8813>  
 Shaida Anwar Kakil  <https://orcid.org/0000-0002-9031-6521>

## References

- [1] Liu Q, Liu Y, Wu F, Cao X, Li Z, Alharbi M, Abbas A N, Amer M R and Zhou C 2018 Highly sensitive and wearable In<sub>2</sub>O<sub>3</sub> nanoribbon transistor biosensors with integrated on-chip gate for glucose monitoring in body fluids *ACS Nano* **12** 1170–8
- [2] Hong S et al 2019 Humidity-sensitive field effect transistor with In<sub>2</sub>O<sub>3</sub> nanoparticles as a sensing layer *J. Nanosci. Nanotechnol.* **19** 6656–62
- [3] Li C, Zhang D, Liu X, Han S, Tang T, Han J and Zhou C 2003 In<sub>2</sub>O<sub>3</sub> nanowires as chemical sensors *Appl. Phys. Lett.* **82** 1613–5
- [4] Su M, Zou X, Gong Y, Wang J, Liu Y, Ho J C, Liu X and Liao L 2018 Sub-kT/q switching in In<sub>2</sub>O<sub>3</sub> nanowire negative capacitance field-effect transistors *Nanoscale* **10** 19131–9
- [5] Zhang H, Meng Y, Song L, Luo L, Qin Y, Han N, Yang Z, Liu L, Ho J C and Wang F 2018 High-performance enhancement-mode thin-film transistors based on Mg-doped In<sub>2</sub>O<sub>3</sub> nanofiber networks *Nano Res.* **11** 1227–37
- [6] Lee J, Moon J, Pi J-E, Ahn S-D, Oh H, Kang S-Y and Kwon K-H 2018 High mobility ultra-thin crystalline indium oxide thin film transistor using atomic layer deposition *Appl. Phys. Lett.* **113** 112102
- [7] Faber H, Lin Y-H, Thomas S R, Zhao K, Pliatsikas N, McLachlan M A, Amassian A, Patsalas P A and Anthopoulos T D 2015 Indium oxide thin-film transistors processed at low temperature via ultrasonic spray pyrolysis *ACS Appl. Mater. Interfaces* **7** 782–90
- [8] Veeraswamy Y, Vijayakumar Y and Reddy M R 2014 Effect of substrate on structural and optical properties of In<sub>2</sub>O<sub>3</sub> thin films prepared by electron beam evaporation *Asian J. Appl. Sci.* **7** 737–44
- [9] Zhu L, He G, Lv J, Fortunato E and Martins R 2018 Fully solution-induced high performance indium oxide thin film transistors with ZrOx high-k gate dielectrics *RSC Adv.* **8** 16788–99
- [10] Park J W, Kang B H and Kim H J 2019 A review of low-temperature solution-processed metal oxide thin-film transistors for flexible electronics *Adv. Funct. Mater.* **30** 1904632
- [11] Kim J, Rim Y S, Chen H, Cao H H, Nakatsuka N, Hinton H L, Zhao C, Andrews A M, Yang Y and Weiss P S 2015 Fabrication of high-performance ultrathin In<sub>2</sub>O<sub>3</sub> film field-effect transistors and biosensors using chemical lift-off lithography *ACS Nano* **9** 4572–82
- [12] Nayak P K et al 2013 High performance In<sub>2</sub>O<sub>3</sub> thin film transistors using chemically derived aluminum oxide dielectric *Appl. Phys. Lett.* **103** 033518
- [13] Zhang H Z, Cao H T, Chen A H, Liang L Y, Liu Z M and Wan Q 2010 Enhancement of electrical performance in In<sub>2</sub>O<sub>3</sub> thin-film transistors by improving the densification and surface morphology of channel layers *Solid State Electron.* **54** 479–83
- [14] Noh J H et al 2010 Indium oxide thin-film transistors fabricated by RF sputtering at room temperature *IEEE Electron Device Lett.* **31** 567–9
- [15] Han Kang D, Ung Han J, Mativenga M, Hwa Ha S and Jang J 2013 Threshold voltage dependence on channel length in amorphous-indium-gallium-zinc-oxide thin-film transistors *Appl. Phys. Lett.* **102** 083508
- [16] Lan L, Xu M, Peng J, Xu H, Li M, Luo D, Zou J, Tao H, Wang L and Yao R 2011 Influence of source and drain contacts on the properties of the indium-zinc oxide thin-film transistors based on anodic aluminum oxide gate dielectrics *J. Appl. Phys.* **110** 103703
- [17] Walsh A et al 2008 Nature of the band gap of In<sub>2</sub>O<sub>3</sub> revealed by first-principles calculations and x-ray spectroscopy *Phys. Rev. Lett.* **100** 167402
- [18] Yuan Z, Zhu X, Wang X, Cai X, Zhang B, Qiu D and Wu H 2011 Annealing effects of In<sub>2</sub>O<sub>3</sub> thin films on electrical properties and application in thin film transistors *Thin Solid Films* **519** 3254–8
- [19] Wang C, Meng Y, Guo Z, Shin B, Liu G and Shan F 2018 High-performance field-effect transistors based on gadolinium doped indium oxide nanofibers and their application in logic gate *Appl. Phys. Lett.* **112** 213501
- [20] Keller J, Stolt L, Edoff M and Törndahl T 2016 Atomic layer deposition of In<sub>2</sub>O<sub>3</sub> transparent conductive oxide layers for application in Cu (In, Ga)Se<sub>2</sub> solar cells with different buffer layers *Phys. Status Solidi a* **213** 1541–52
- [21] Agbenyeke R E, Jung E A, Park B K, Chung T-M, Kim C G and Han J H 2017 Thermal atomic layer deposition of In<sub>2</sub>O<sub>3</sub> thin films using dimethyl (N-ethoxy-2, 2-dimethylcarboxylicpropanamide) indium and H<sub>2</sub>O *Appl. Surf. Sci.* **419** 758–63
- [22] Matsui H and Tabata H 2019 Assembled films of Sn-doped In<sub>2</sub>O<sub>3</sub> plasmonic nanoparticles on high-permittivity substrates for thermal shielding *ACS Appl. Nano Mater.* **2** 2806–16
- [23] Veeraswami Y et al Structural and electrical properties of In<sub>2</sub>O<sub>3</sub> thin films prepared by pulsed laser deposition *AIP Conf. Proc.* **2018** 1942 08003
- [24] Vygranenko Y, Wang K and Nathan A 2007 Stable indium oxide thin-film transistors with fast threshold voltage recovery *Appl. Phys. Lett.* **91** 263508
- [25] Suresh A and Muth J 2008 Bias stress stability of indium gallium zinc oxide channel based transparent thin film transistors *Appl. Phys. Lett.* **92** 033502

- [26] Lin Y H *et al* 2015 High Electron mobility thin-film transistors based on solution-processed semiconducting metal oxide heterojunctions and quasi-superlattices *Adv. Sci.* **2** 1500058
- [27] Nomura K, Kamiya T, Hirano M and Hosono H 2009 Origins of threshold voltage shifts in room-temperature deposited and annealed a-In–Ga–Zn–O thin-film transistors *Appl. Phys. Lett.* **95** 013502
- [28] Lee J-M, Cho I-T, Lee J-H and Kwon H-I 2008 Bias-stress-induced stretched-exponential time dependence of threshold voltage shift in InGaZnO thin film transistors *Appl. Phys. Lett.* **93** 093504
- [29] Paine D C, Yaglioglu B, Beiley Z and Lee S 2008 Amorphous IZO-based transparent thin film transistors *Thin Solid Films* **516** 5894–8
- [30] Choi J H, Han U B, Lee K C, Lee J-H, Kim -J-J, Cho I-T, Lee J-H and Heo Y-W 2009 Transfer characteristics and bias-stress stability of amorphous indium zinc oxide thin-film transistors *J. Vac. Sci. Technol. B* **27** 622–5
- [31] Kaftanoglu K, Venugopal S M, Marrs M, Dey A, Bawolek E J, Allee D R and Loy D 2011 Stability of IZO and a-Si: H TFTs processed at low temperature *J. Disp. Technol.* **7** 339–43
- [32] Cross R and De Souza M 2006 Investigating the stability of zinc oxide thin film transistors *Appl. Phys. Lett.* **89** 263513
- [33] Young N and Gill A 1990 Electron trapping instabilities in polycrystalline silicon thin film transistors *Semicond. Sci. Technol.* **5** 72
- [34] Zafar S, Callegari A, Gusev E and Fischetti M V 2003 Charge trapping related threshold voltage instabilities in high permittivity gate dielectric stacks *J. Appl. Phys.* **93** 9298–303
- [35] Berberan-Santos M, Bodunov E and Valeur B 2005 Mathematical functions for the analysis of luminescence decays with underlying distributions 1. Kohlrausch decay function (stretched exponential) *Chem. Phys.* **315** 171–82
- [36] Shih -C-C, Lee Y-S, Fang K-L, Chen C-H and Gan F-Y 2007 A current estimation method for bias-temperature stress of a-Si TFT device *IEEE Trans. Device Mater. Reliab.* **7** 347–50
- [37] Kim J I *et al* 2015 Local-degradation-induced threshold voltage shift in turned-off amorphous InGaZnO thin film transistors under AC drain bias stress *IEEE Electron Device Lett.* **36** 579–81
- [38] Li J, Lu L, Chen R, Kwok H-S and Wong M 2017 A physical model for metal–oxide thin-film transistor under gate-bias and illumination stress *IEEE Trans. Electron Devices* **65** 142–9
- [39] Kim Y, Ha T-K, Cho Y-J, Kang Y-S, Yu S, Kim G, Jeong H, Park J K and Kim O 2020 Severe hump phenomenon induced by increased charge trapping and suppression of electron capture effect in amorphous In–Ga–Zn–O thin-film transistors under unipolar pulsed drain bias with static positive gate bias stress *Solid State Electron.* **167** 107785
- [40] Qian H-M, Yu G, Lu H, Wu C-F, Tang L-F, Zhou D, Ren -F-F, Zhang R, Zheng Y-L and Huang X-M 2015 Temperature-dependent bias-stress-induced electrical instability of amorphous indium-gallium-zinc-oxide thin-film transistors *Chin. Phys. B* **24** 077307
- [41] Lin Y-H *et al* 2019 Hybrid organic–metal oxide multilayer channel transistors with high operational stability *Nat. Electron.* **2** 587–95
- [42] Lee H, Kwon J-H, Bae J-H, Park J and Seo C 2019 Electrical stability of solution-processed indium oxide thin-film transistors *J. Nanosci. Nanotechnol.* **19** 2371–4
- [43] Okamura K and Hahn H 2010 Carrier transport in nanocrystalline field-effect transistors: impact of interface roughness and geometrical carrier trap *Appl. Phys. Lett.* **97** 153114
- [44] Merticaru A R, Mouthaan A J and Kuper F G 2006 Current degradation of a-Si: H/SiN TFTs at room temperature and low voltages *IEEE Trans. Electron Devices* **53** 2273–9
- [45] Libsch F and Kanicki J 1993 Bias-stress-induced stretched-exponential time dependence of charge injection and trapping in amorphous thin-film transistors *Appl. Phys. Lett.* **62** 1286–8